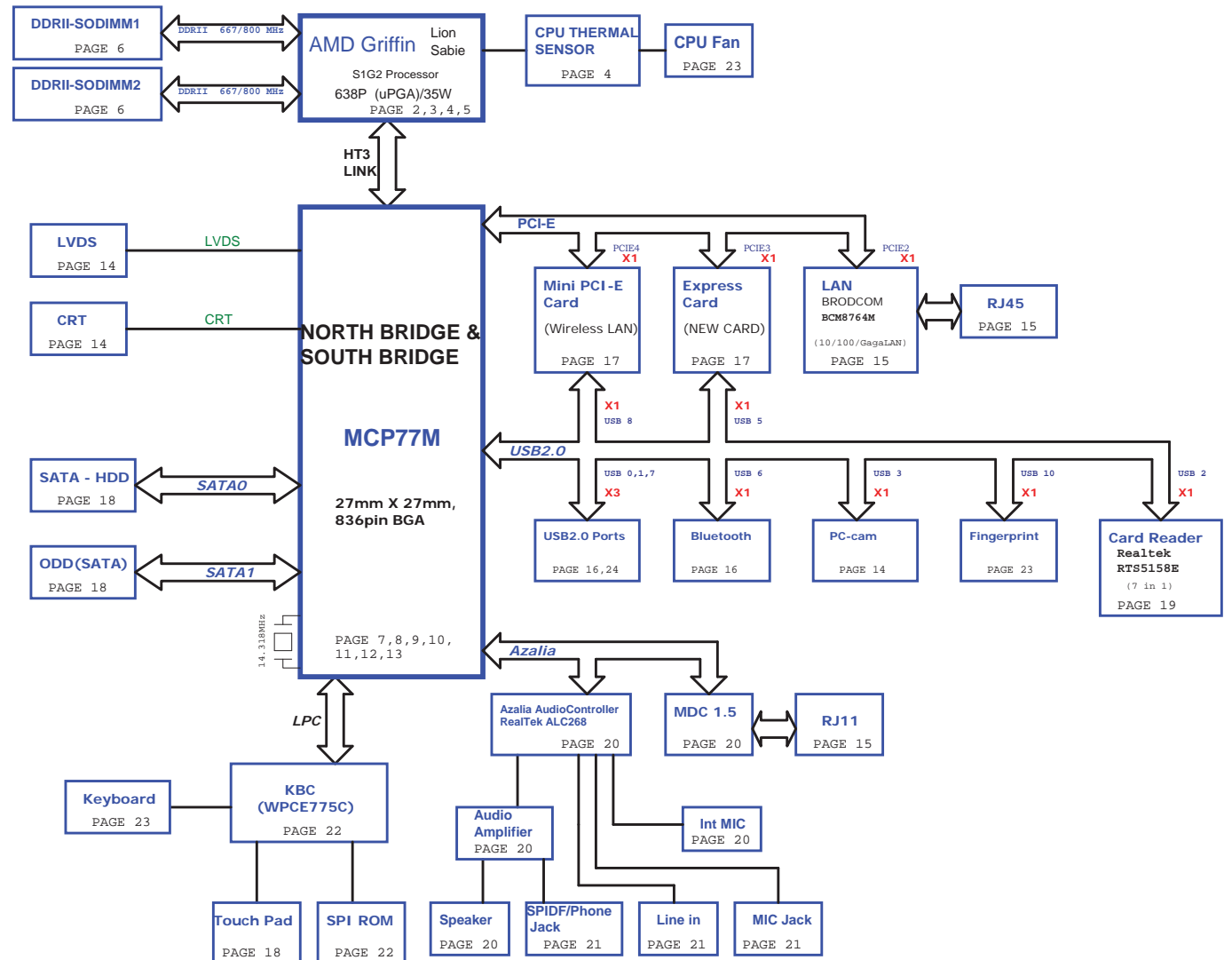


Z05 SYSTEM BLOCK DIAGRAM



CPU CORE / VDDNB (ISL6265A)	PAGE 26
NB_CORE +1.1V (RT8202)	PAGE 28
+1.1V_NB (RT8202)	PAGE 27
DDR II SMDRR_VTERM 1.8VSUS(TPSS1116REGR)	PAGE 29
SYSTEM POWER (ISL6237)	PAGE 25
SYSTEM CHARGER (ISL6251A)	PAGE 24



PCB STACK UP

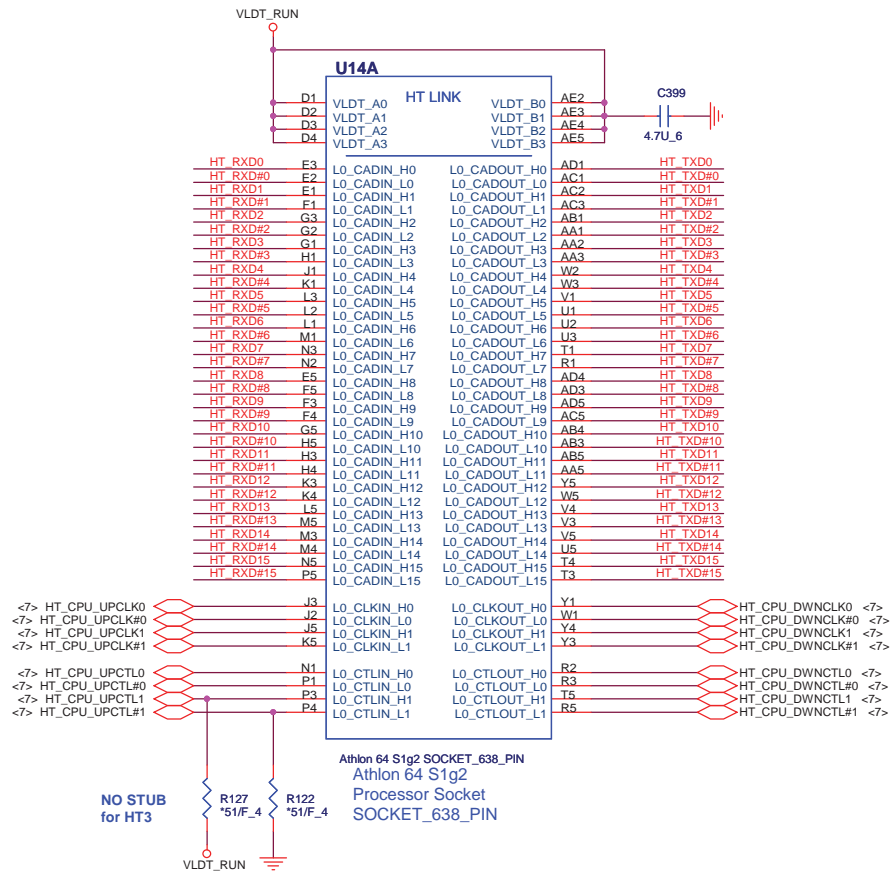
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

<7> HT_RXD#[15..0] HT_RXD[15..0]
 <7> HT_TXD#[15..0] HT_TXD[15..0]

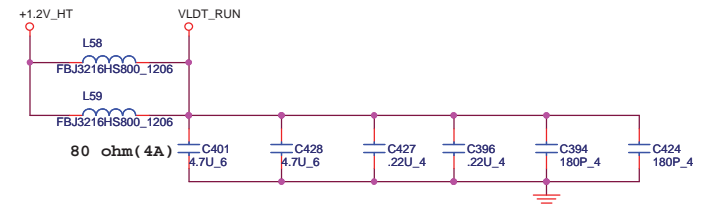


PROCESSOR HYPERTRANSPORT INTERFACE

VLDLT_Ax AND VLDLT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



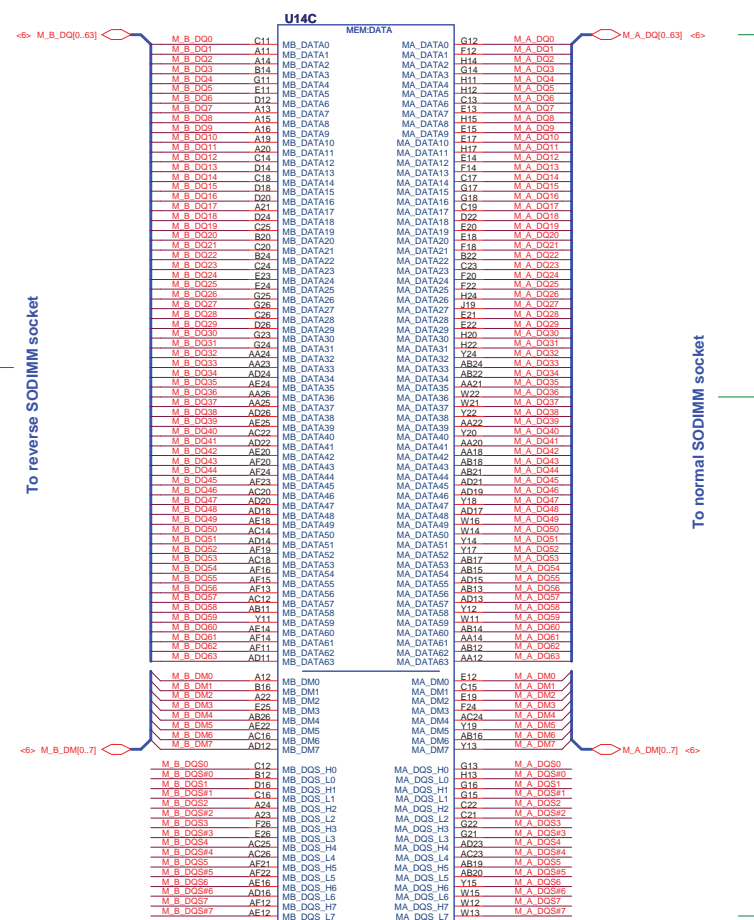
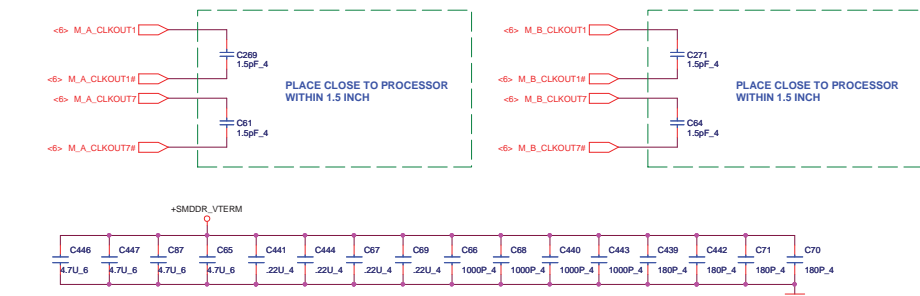
Note: on MCP77, (HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.



LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDLT0 POWER PINS

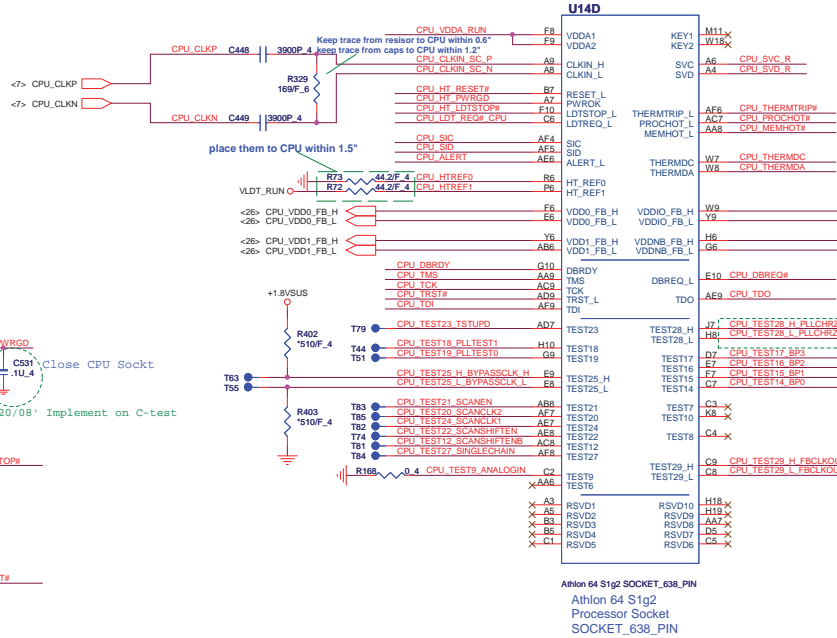
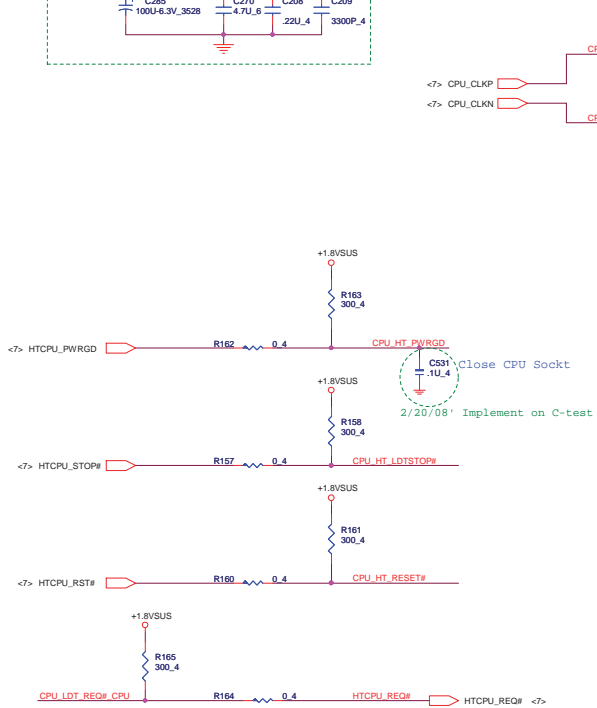
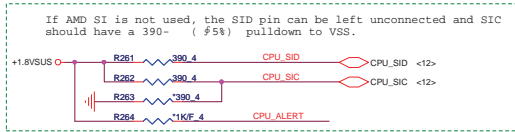
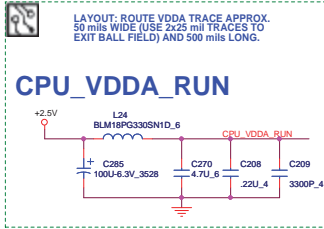
		Quanta Computer Inc. PROJECT : Z05	
		Size	Document Number
AMD Griffin HT I/F		Rev	1A
Date:	Monday, February 25, 2008	Sheet	2 of 34



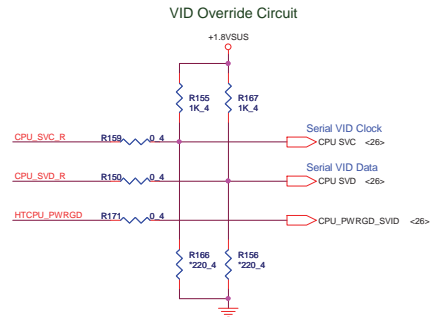
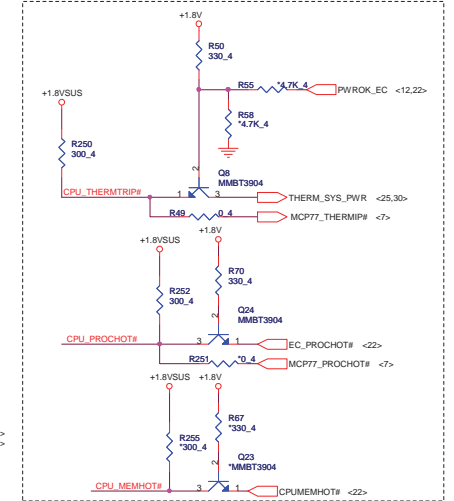
To normal SODIMM socket



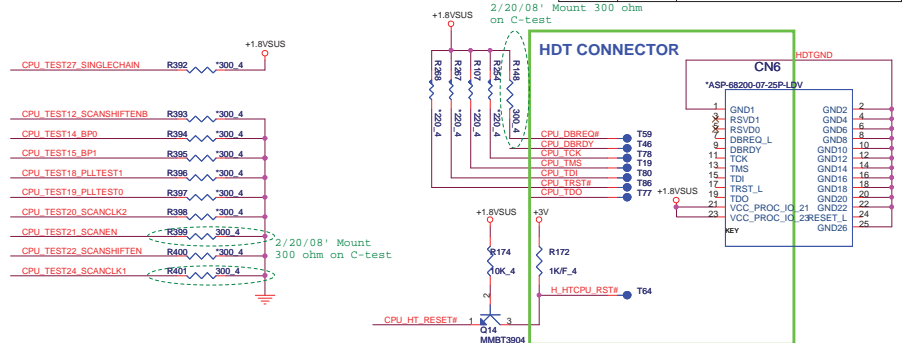
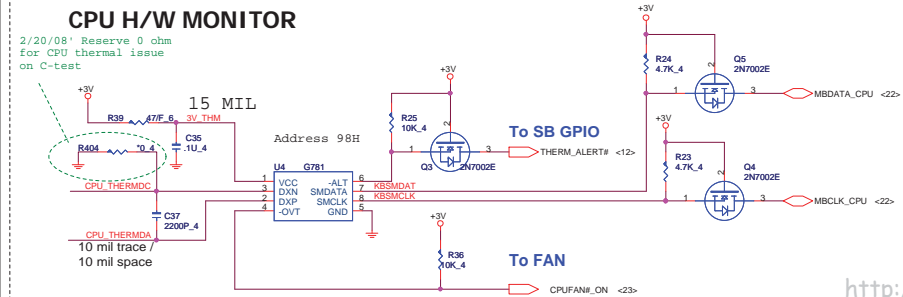
ATHLON Control and Debug



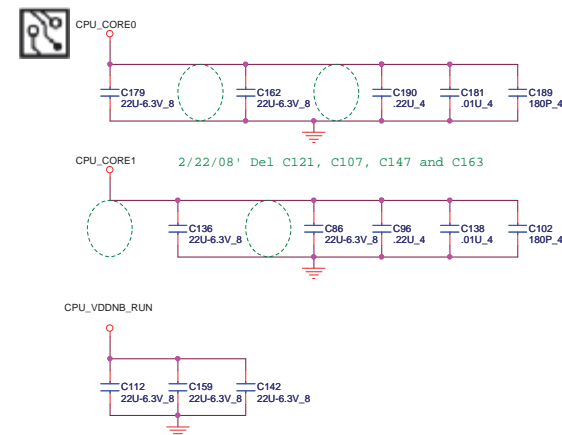
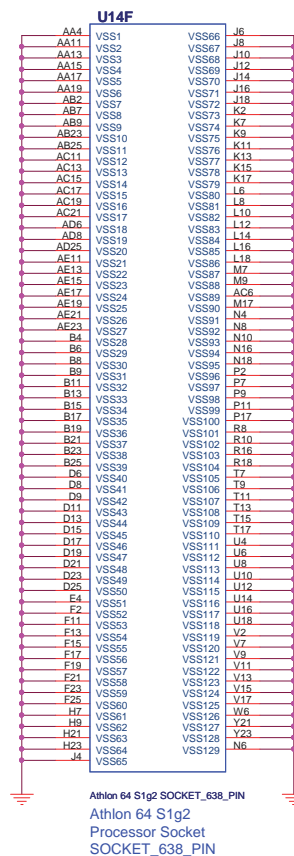
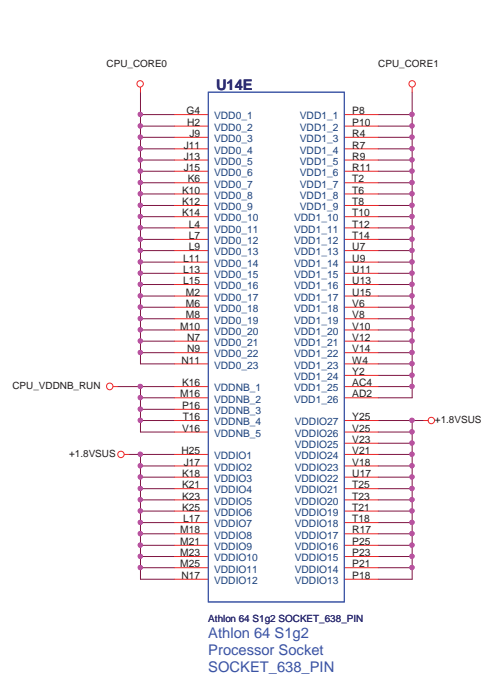
Athlon 64 S1g2 SOCKET_638_PIN



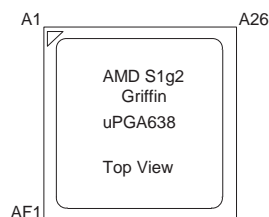
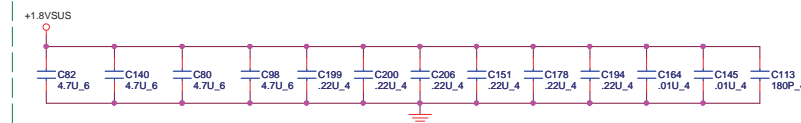
SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

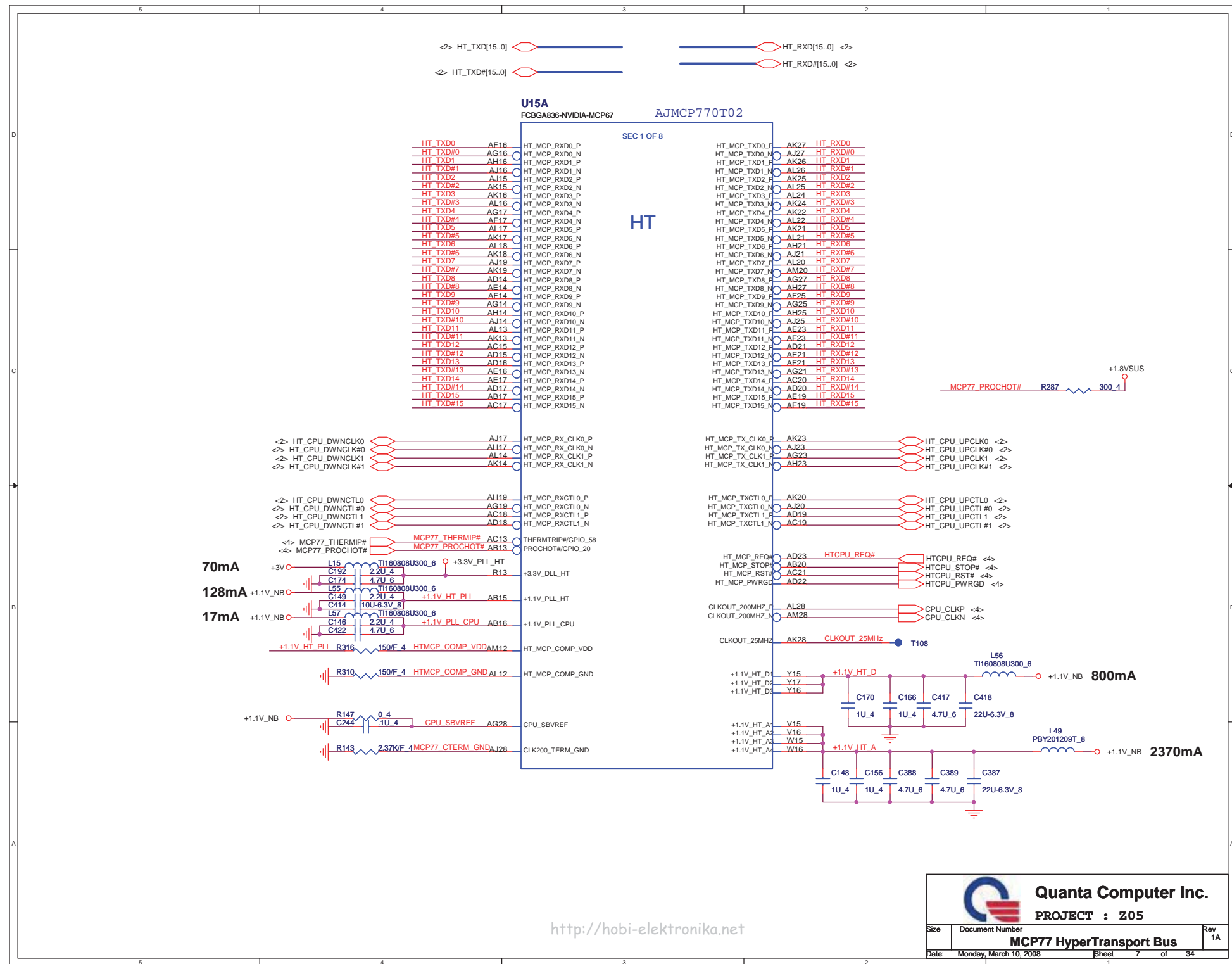


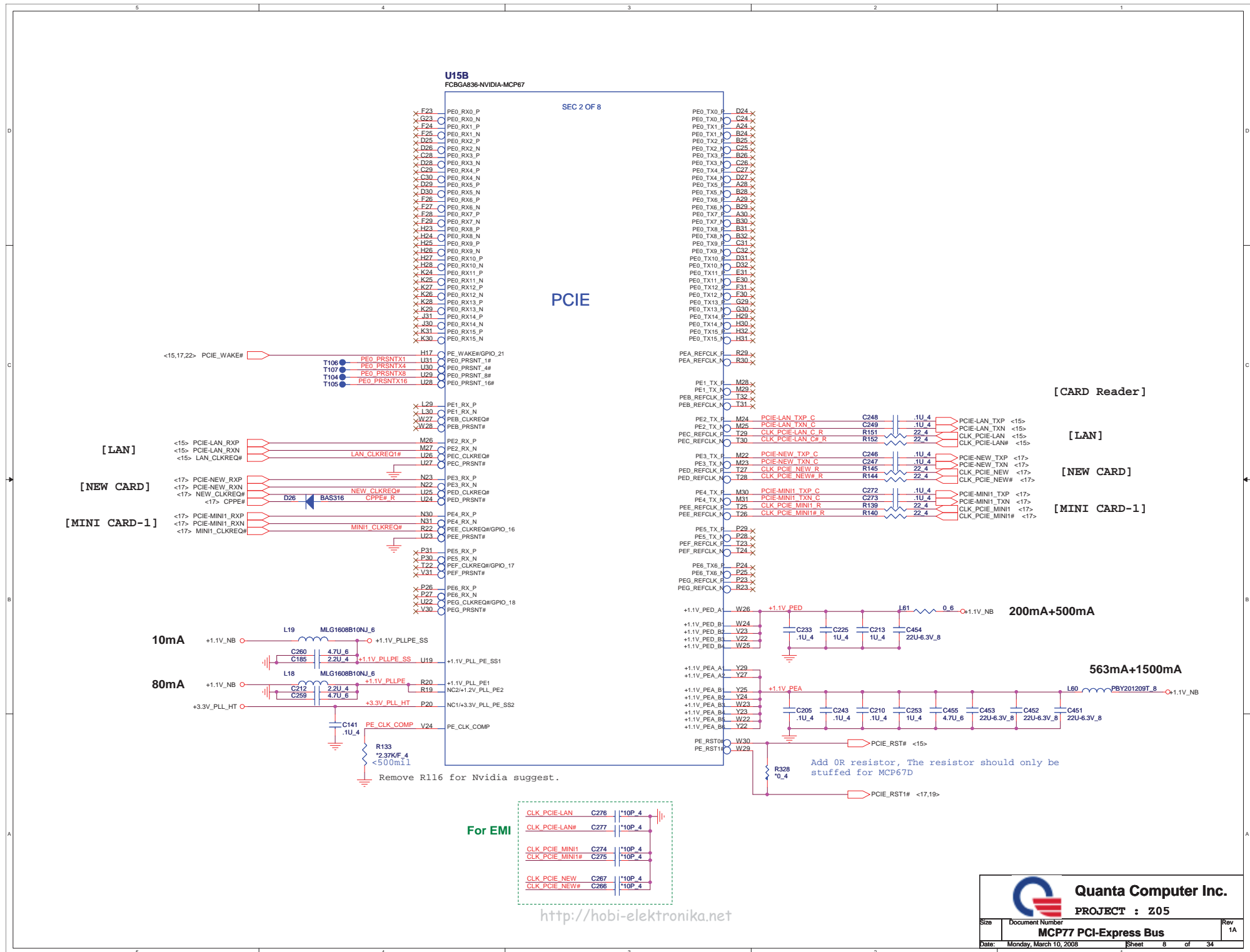
PROCESSOR POWER AND GROUND



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE







U15D

FCBGA836-NVIDIA-MCP67

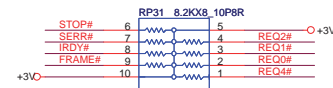
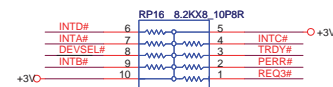
PCI

MCP77

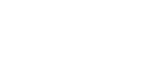
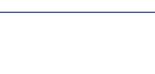
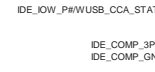
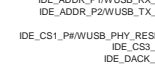
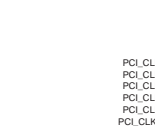
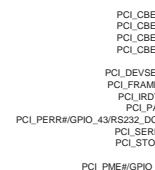
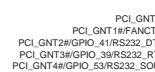
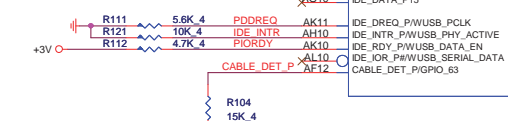
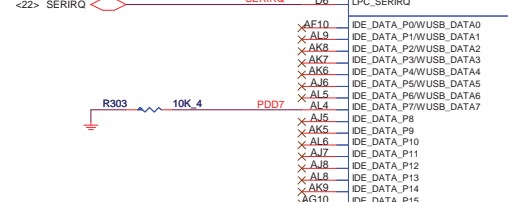
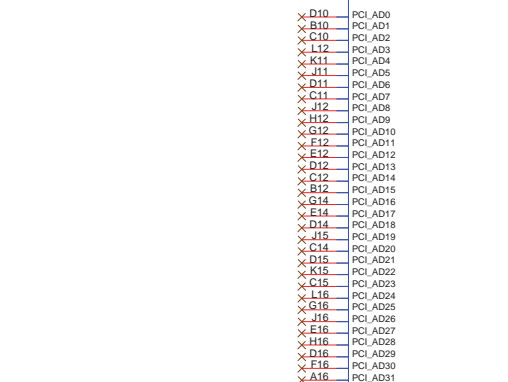
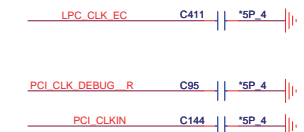
LPC

IDE

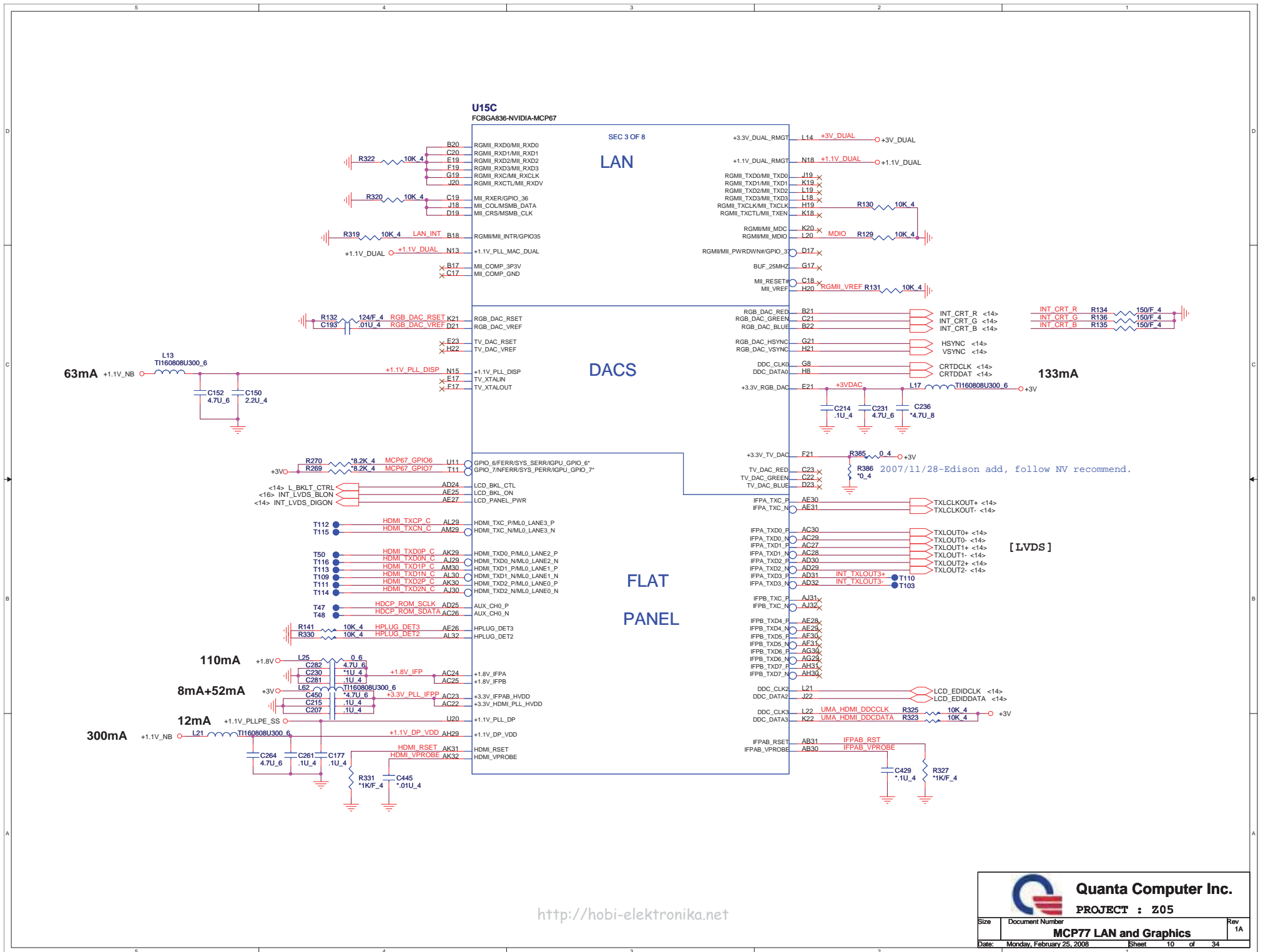
PCI/LPC PULL-UP

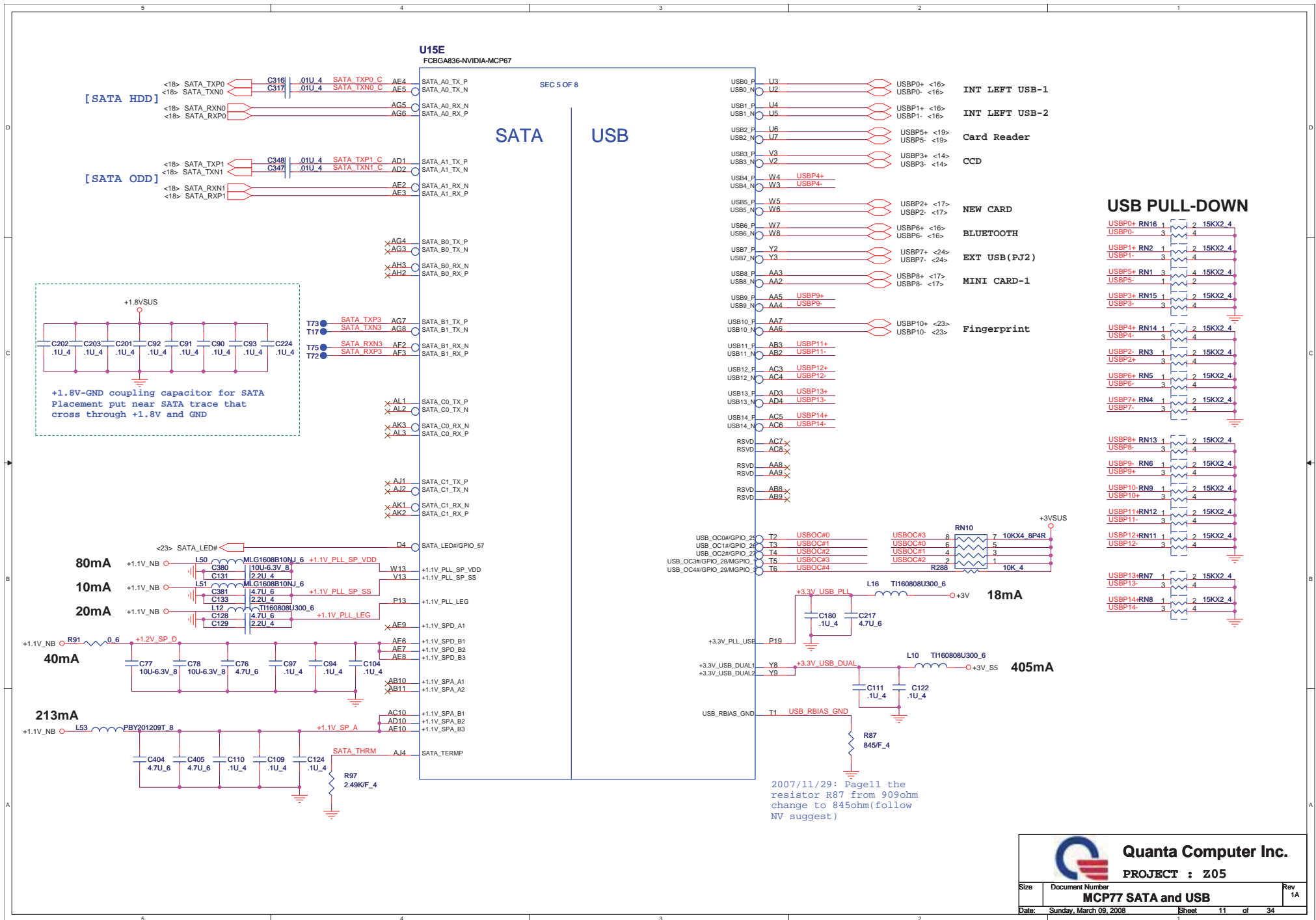


CLOCK BYPASS



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U15F FCBGA36-NVIDIA-MCP67

HDA

MISC

HDA

HDA_SDOUT	R74	22 4	HDA_SDOUT_ADO	<20>
HDA_SYNC	R77	22 4	HDA_SYNC_MDC	<20>
HDA_BITCLK	R285	22 4	HDA_SYNC_ADO	<20>
HDA_RESET#	R292	22 4	HDA_SYNC_MDC	<20>
	R81	22 4	HDA_BITCLK_ADO	<20>
	R86	22 4	HDA_RESET#_ADO	<20>
	R284	22 4	HDA_RESET#_MDC	<20>
	R291	22 4		

EMI Solution

HDA_SDOUT	C373	10P 4
HDA_SYNC	C395	10P 4
HDA_RESET#	C393	10P 4
HDA_BITCLK	C392	10P 4

MCP77 STRAPPING

HDA_RESET# (LAN)	0	MI
HDA_RESET# (LAN)	1	RGMI (DEFAULT)
HDA_RESET# (LAN)	2	RGMI (DEFAULT)
HDA_RESET# (LAN)	3	RGMI (DEFAULT)
HDA_RESET# (LAN)	4	RGMI (DEFAULT)
HDA_RESET# (LAN)	5	RGMI (DEFAULT)
HDA_RESET# (LAN)	6	RGMI (DEFAULT)
HDA_RESET# (LAN)	7	RGMI (DEFAULT)
HDA_RESET# (LAN)	8	RGMI (DEFAULT)
HDA_RESET# (LAN)	9	RGMI (DEFAULT)
HDA_RESET# (LAN)	10	RGMI (DEFAULT)
HDA_RESET# (LAN)	11	RGMI (DEFAULT)

MCP SPKR (Boot MODE)

0	USER TABLE (DEFAULT)
1	SAFE TABLE

HDA_SYNC R (SIO CLOCK)

0	14.318MHz (DEFAULT)
1	24MHz

SPI DO SPI CLK (SPI CLOCK)

00	31MHz
01	42MHz
10	25MHz
11	1MHz

3V_S5

R280	10K 4	HDA_RESET#
R293	10K 4	

R273	8.2K 4	HDA_SDOUT
R286	8.2K 4	

R113	8.2K 4	LFRAME# <9,17,22>
R114	8.2K 4	

R95	10K 4	MCP SPKR
R96	10K 4	

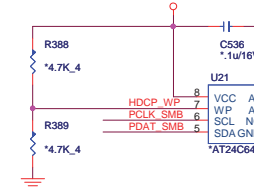
R78	10K 4	HDA_SYNC
R295	10K 4	

R299	10K 4	MCP SPI DO
R290	10K 4	

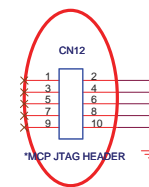
R298	10K 4	MCP SPI CLK
R289	10K 4	

Acer Suggest Reserve HDCP EEPROM 2007/12/05

HDCP EEPROM



NO PN



M/B ID for 14"/17"

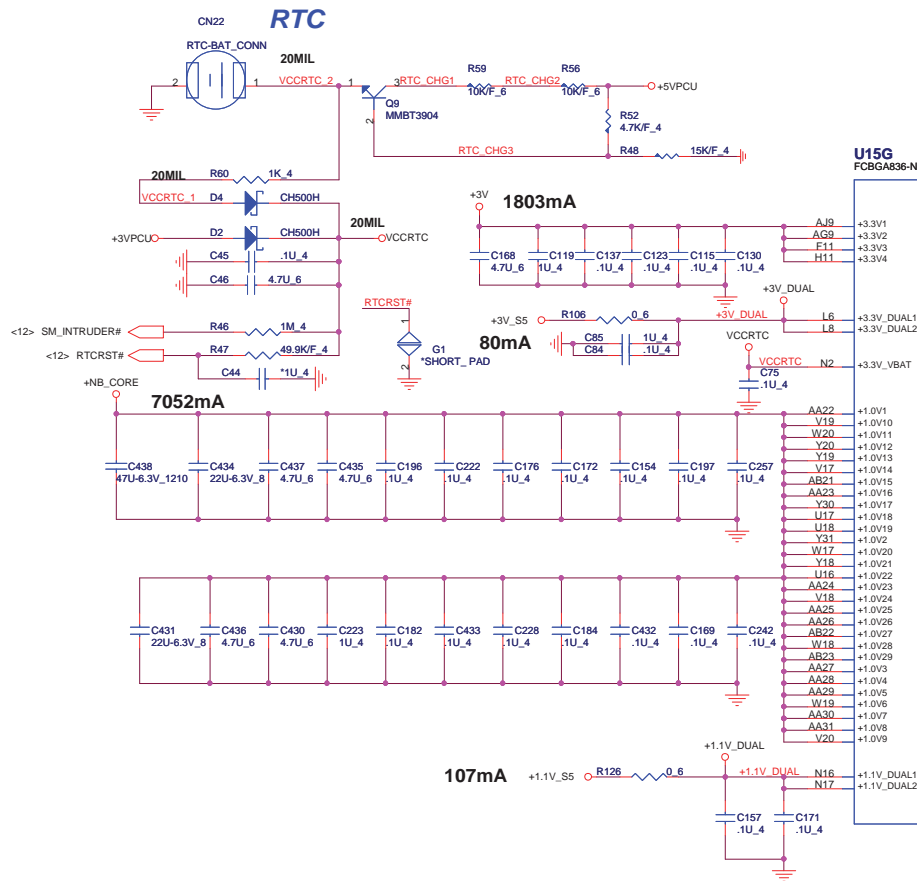
ID0	ID1	ID2	M/B
0	0	0	17" D
0	0	1	X
0	1	0	15" D
1	0	0	15" U
1	0	1	14" Dual Core CPU & MXM
1	1	0	14" Dual Core CPU & UMA
1	1	1	14" Single Core CPU & UMA

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Quanta Computer Inc.
PROJECT : Z05

Size	Document Number	Rev
	MCP77 HDA/SMB/PMU/GPIO	1A
Date:	Sunday, March 08, 2008	Sheet 12 of 34

MCP77 POWER PLANE/GND & BYPASS



U15G
FCBGA836-NVIDIA-MCP67

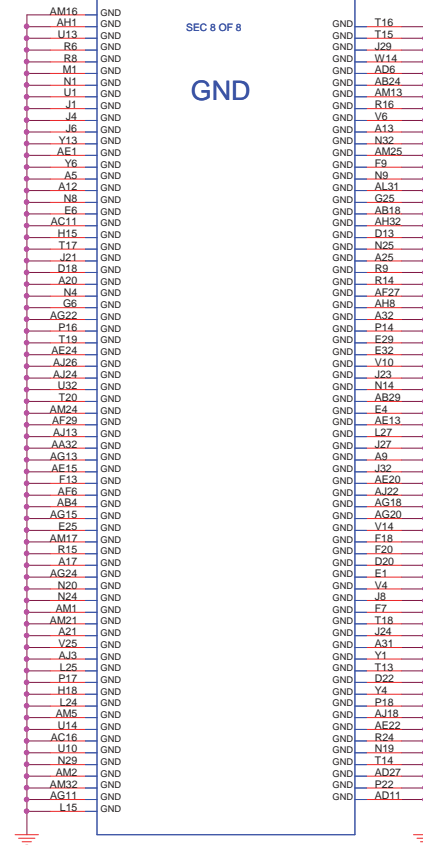
SEC 7 OF 8

PWR/GND

U15H
FCBGA836-NVIDIA-MCP67

SEC 8 OF 8

GND



Quanta Computer Inc.

PROJECT : Z05

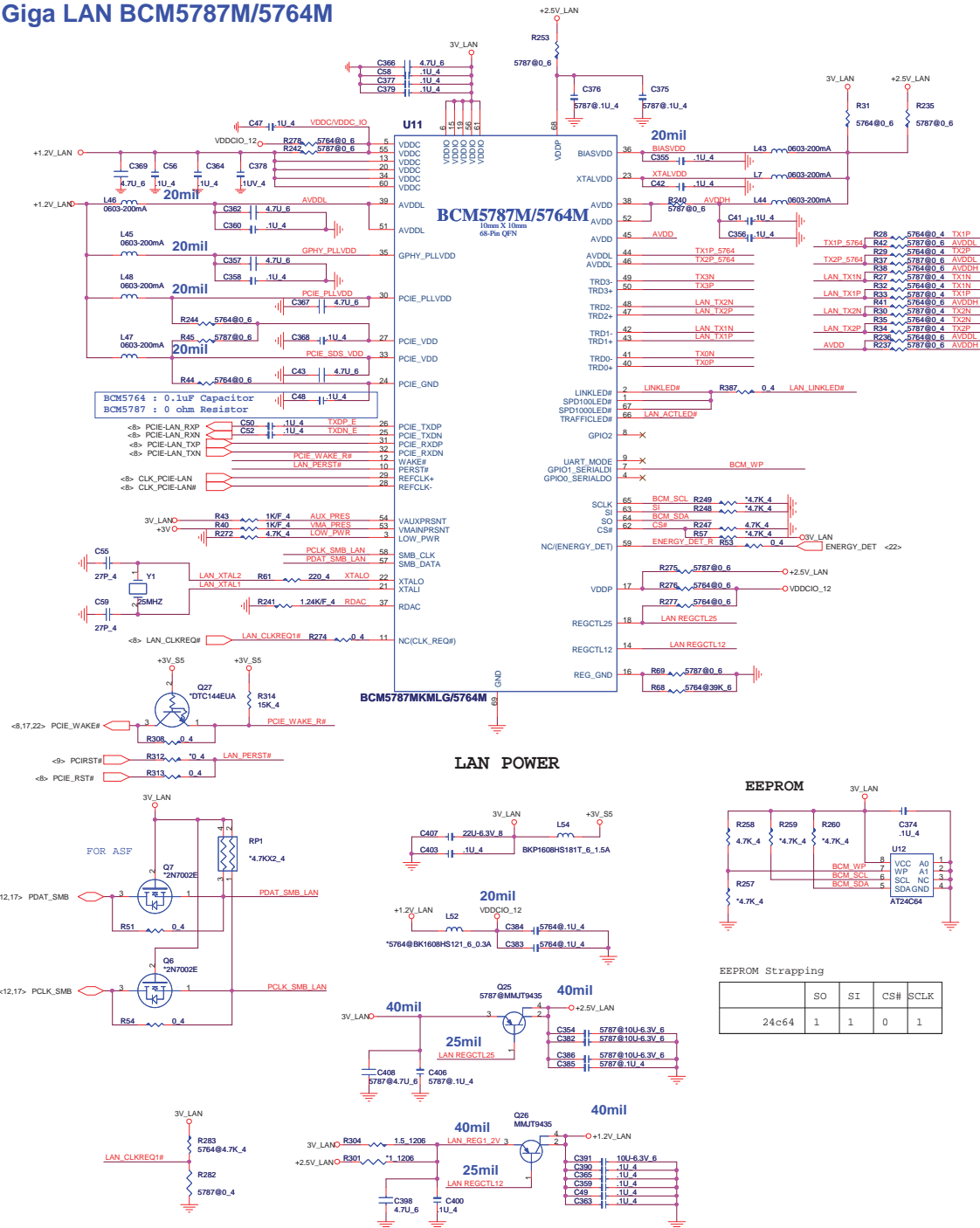
Size	Document Number	Rev
	MCP77 POWER/GND/RTC	1A
Date:	Monday, February 25, 2008	Sheet 13 of 34

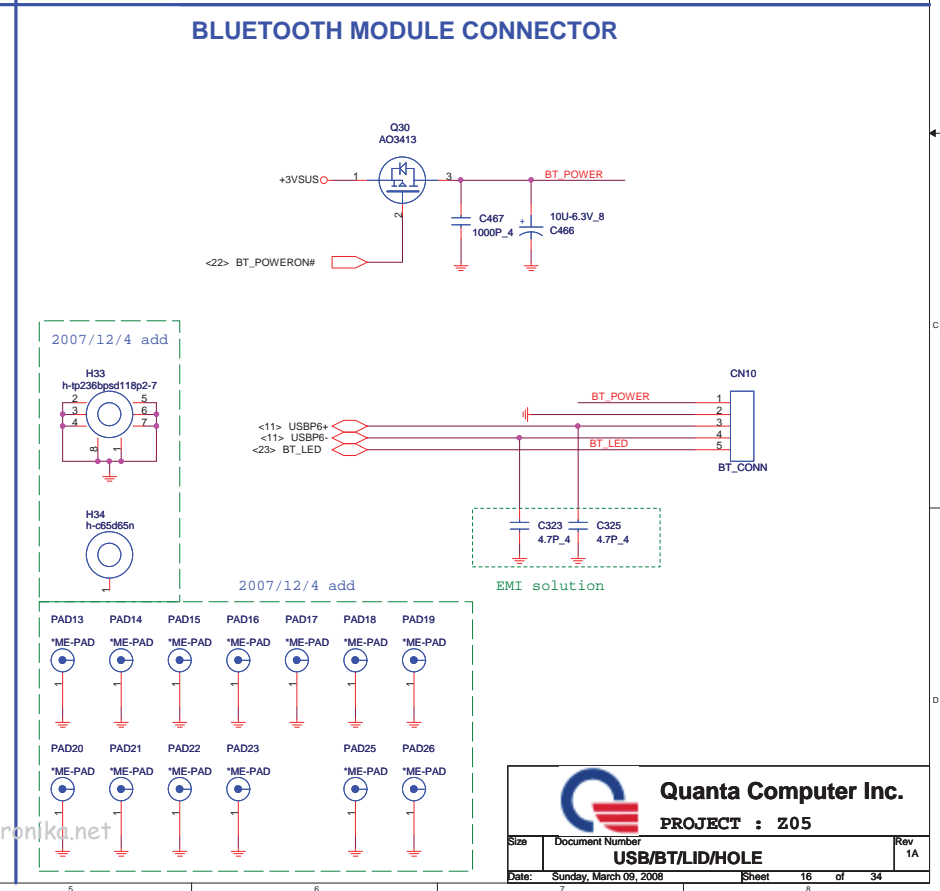
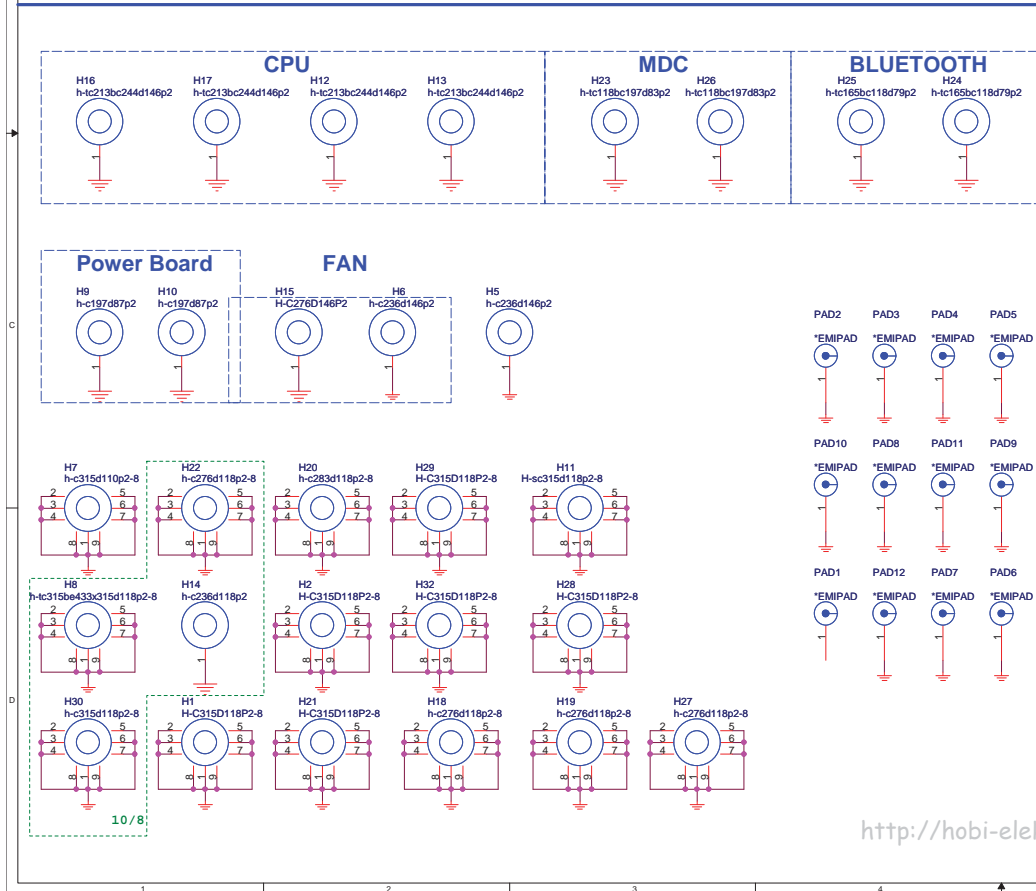
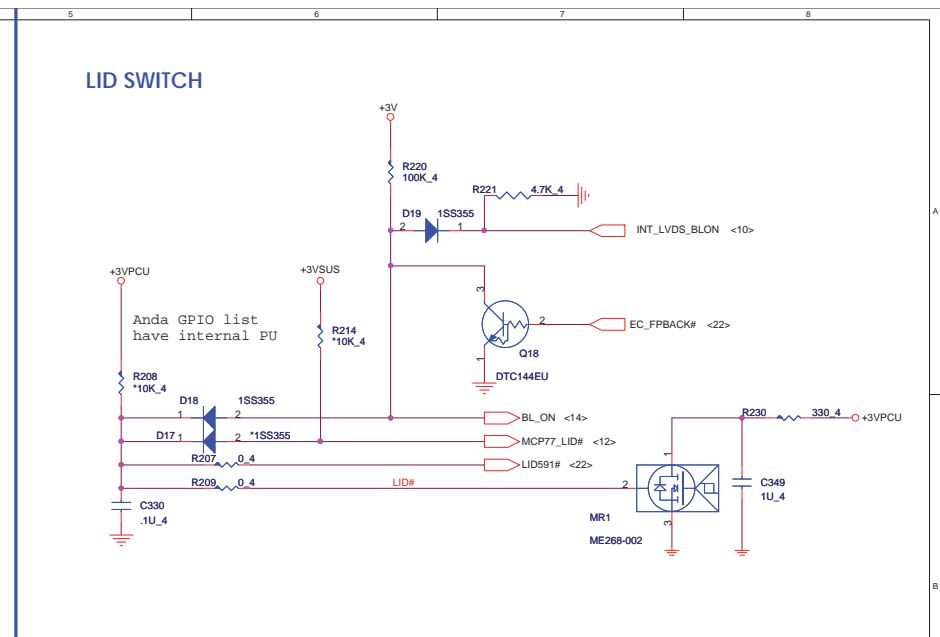
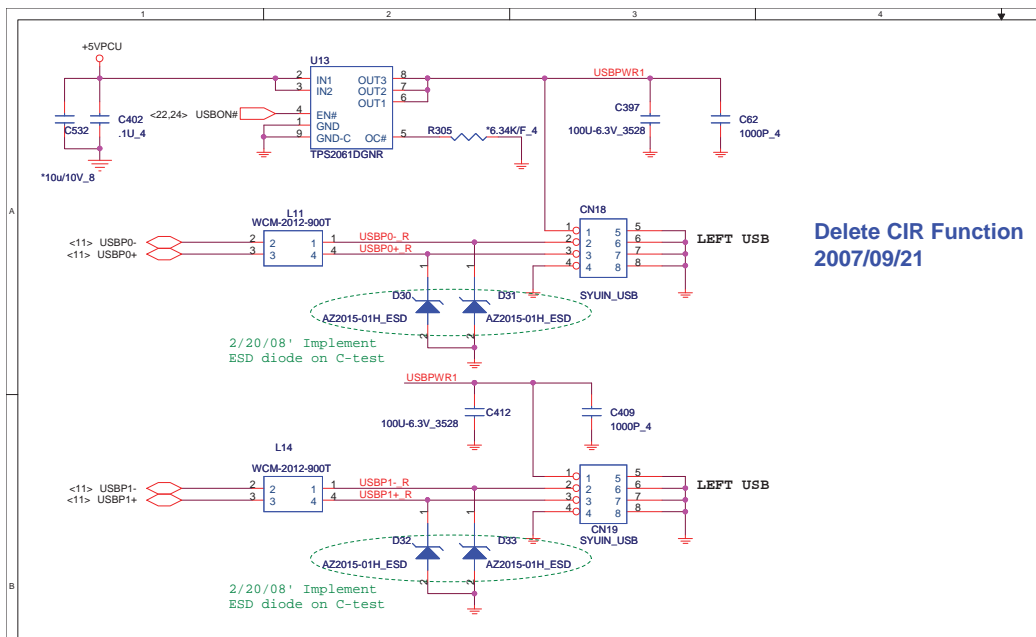
SINGLE_CH



Delete TVOUT MiniDIN

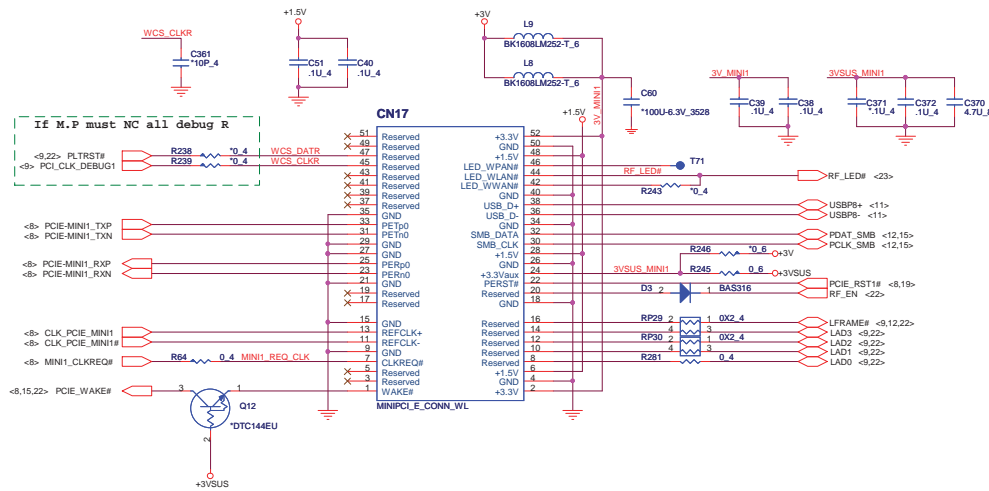
Giga LAN BCM5787M/5764M





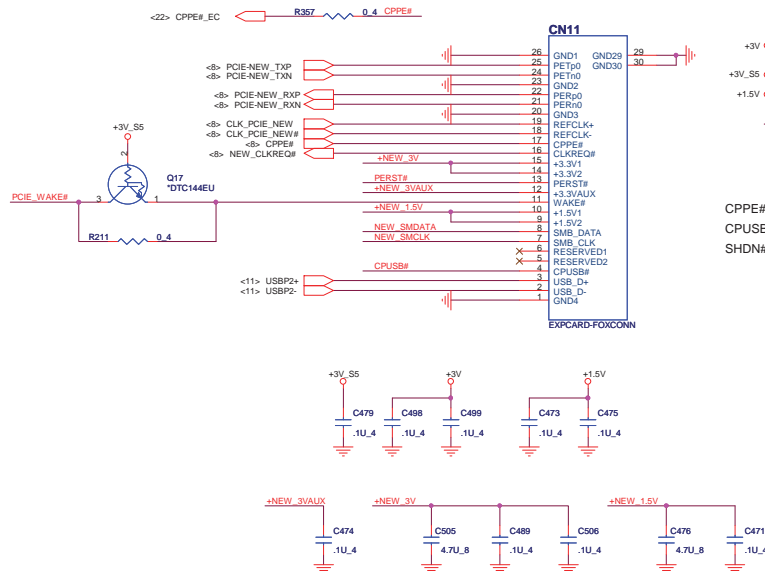
MINI-Card

MINI-Card Port-1

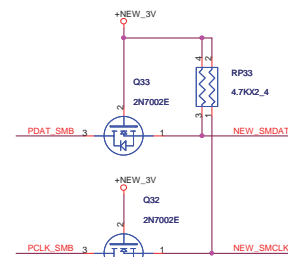
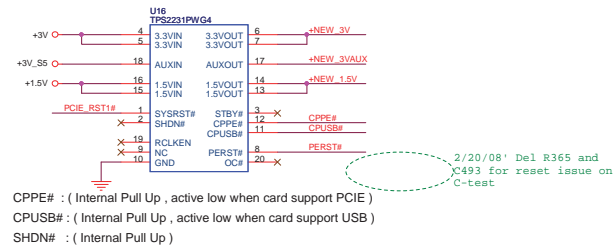


Delete MINI-Card Port-2

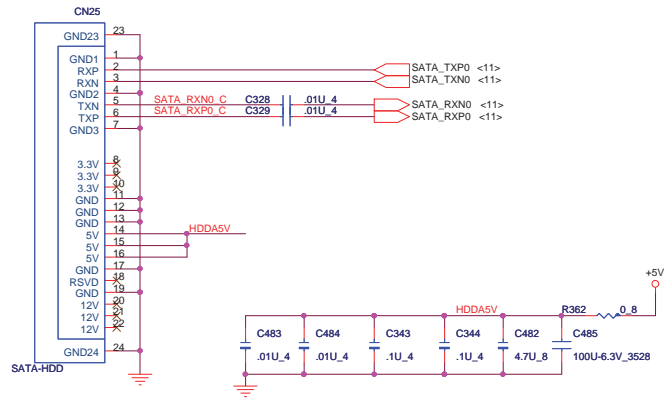
New card



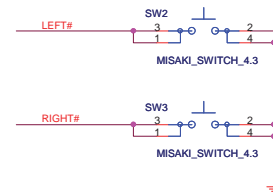
NEW CARD'S POWER SWITCH



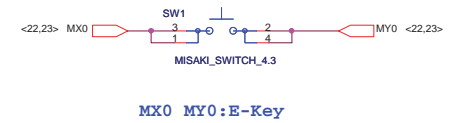
SATA HDD



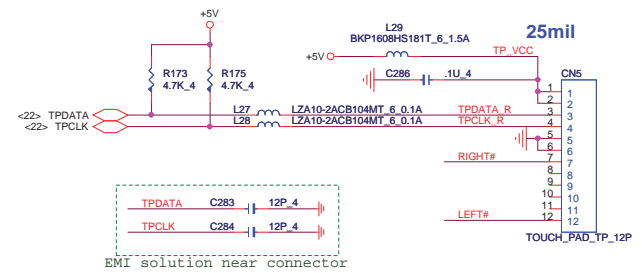
TP SWITCH



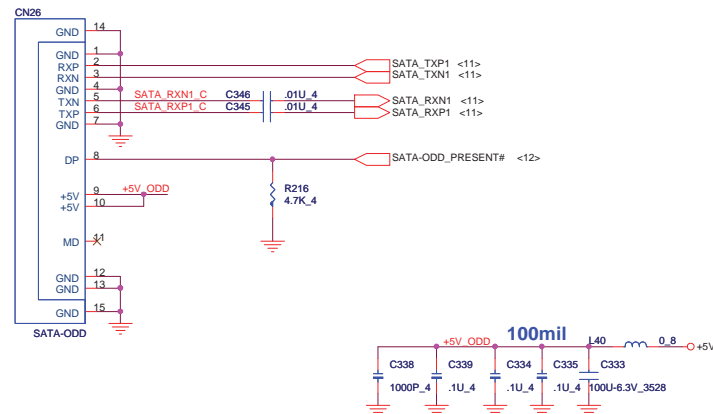
E-KEY



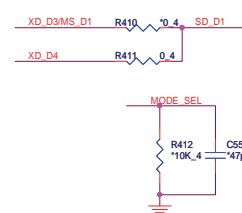
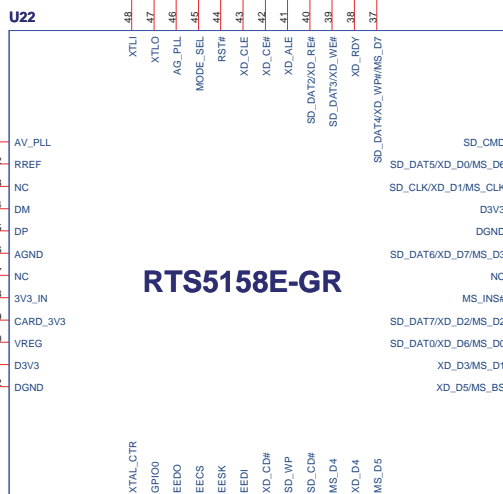
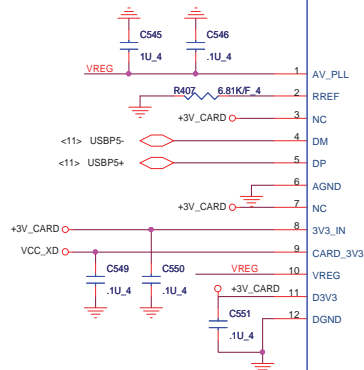
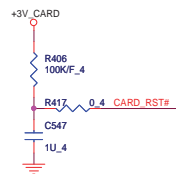
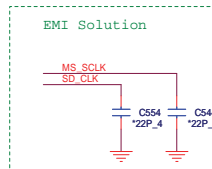
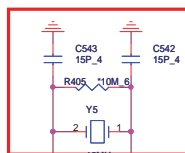
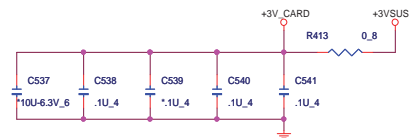
TP CONN



ODD (SATA)

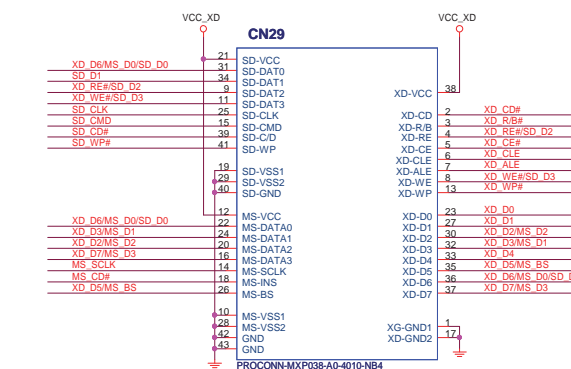
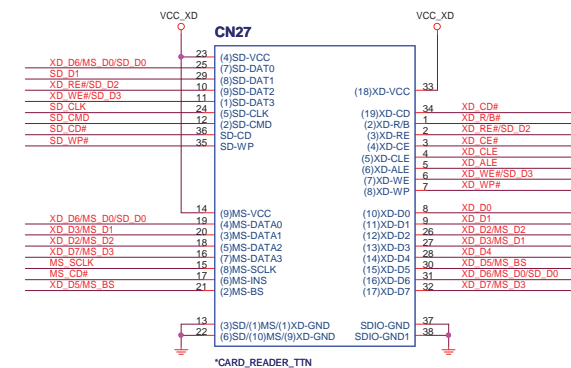


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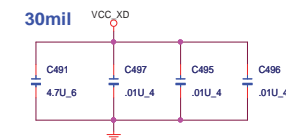


R412/C553 = 10K/47pF => R410 Reside
R412/C553 = NC / NC => R411 Reside

7 IN 1 CARD READER



CARDREADER POWER



The diagram illustrates the electrical interface for the ALC268/ALC888S VC. It shows the connection of the ALC268/ALC888S VC to the HP Jack and various system components. Key components include the HP Jack, ALC268/ALC888S VC, and various passive components like resistors and capacitors. The diagram is divided into several sections: HP Jack, ALC268/ALC888S VC, and various system components. The HP Jack section shows connections for +5V_ADO, SURR-L, SURR-R, and ADOGND. The ALC268/ALC888S VC section shows connections for EAPD, MUTE, and various pins. The system components section shows connections for +3V, +1.5V, +3V0, and various capacitors. The diagram is labeled with component values and pin numbers.

The schematic diagram illustrates the connection of the AD0GND pin for the T201209G121_8_3A component. The circuit is powered by a +5V supply. The T201209G121_8_3A component is connected to the +5V supply via an inductor L38. The output of the T201209G121_8_3A component is connected to the AD0GND pin of the 'G9861-18ADJTEU' component. The AD0GND pin is also connected to the VEN pin of the 'G9861-18ADJTEU' component. The VEN pin is connected to the +5V_ADO supply. The ADJ pin of the 'G9861-18ADJTEU' component is connected to the +5V_ADO supply. The GND pin of the 'G9861-18ADJTEU' component is connected to the GND pin of the 'G9861-18ADJTEU' component. The output of the 'G9861-18ADJTEU' component is connected to the +5V_ADO supply. The circuit also includes capacitors C318, C312, C313, C316, C306, and C309, and resistors R191, R186, and R184.

Vo = 1.2 * (R371 + R372) / R371 = 4.8V

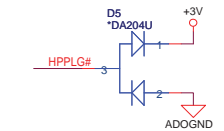
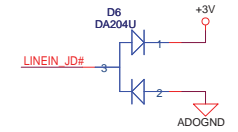
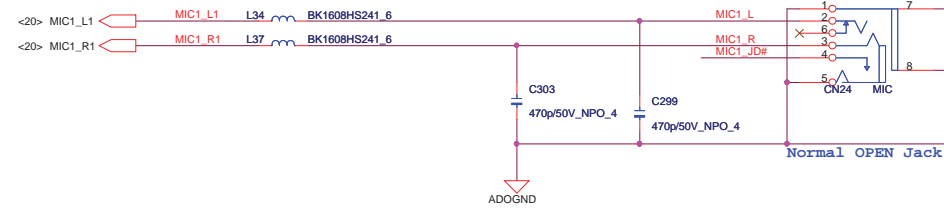
The diagram illustrates the HDA pin connections for the ADI-9635 module. The connections are as follows:

- Pin 1:** Connected to HDA_SDOUT_MDC.
- Pin 2:** Connected to HDA_SYNC_MDC.
- Pin 3:** Connected to HDA_SDI_MDC.
- Pin 4:** Connected to HDA_RESET#_MDC.
- Pin 5:** Connected to GND.
- Pin 6:** Connected to RSV.
- Pin 7:** Connected to AC_SDO.
- Pin 8:** Connected to AC_SYNC.
- Pin 9:** Connected to AC_SDI.
- Pin 10:** Connected to AC_RST#.
- Pin 11:** Connected to AC_BCLK.
- Pin 12:** Connected to HDA_BITCLK_MDC.

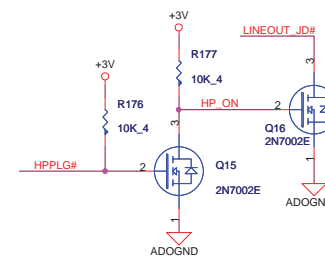
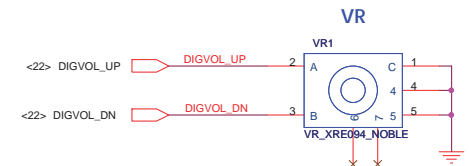
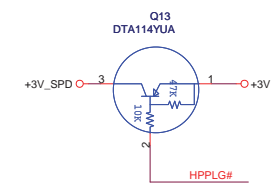
The diagram also shows the connection of the module's internal components to the system ground (GND) and the system power supply (VSSUS). The diagram is labeled "EMI Solution" and "EMI Solution".

SP_S1BY1 (33 pin)	SP_S1BY2 (34 pin)	SP_S1BY ON/OFF
LOW	LOW	ON
LOW	HI	OFF
HI	LOW	OFF
HI	HI	OFF

HP_S1BY1 (35 pin)	HP_S1BY2 (36 pin)	HP_S1BY ON/OFF
LOW	LOW	ON
LOW	HI	OFF
HI	LOW	OFF
HI	HI	OFF

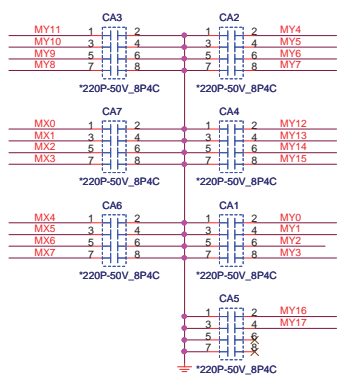
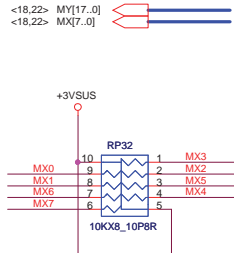


The schematic diagram illustrates the LINEIN signal input circuit. It features two input lines, LINE1-L_1 and LINE1-R_1, which are terminated with 126 ohms and 130 ohms respectively. These lines are connected to a differential input pair of an op-amp. The inputs are also connected to a common-mode feedback network consisting of two 470pF capacitors (C288, C280) connected to ADOGND. The op-amp output is connected to a normal open jack through a 50 ohm resistor (CN23).

[illegible]

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CN4		
1	1	MY0
2	2	MY1
3	3	MY2
4	4	MY3
5	5	MY4
6	6	MY5
7	7	MY6
8	8	MY7
9	9	MY8
10	10	MY9
11	11	MY10
12	12	MY11
13	13	MY12
14	14	MY13
15	15	MY14
16	16	MY15
17	17	MY16
18	18	MY17
19	19	MX7
20	20	MX6
21	21	MX5
22	22	MX4
23	23	MX3
24	24	MX2
25	25	MX1
26	26	MX0



2/21/08' Change from 330ohm
to 220ohm on C-test

+3VPCU

R227 220 4

R229 220 4

R226 220 4

R228 220 4

LED1
LED_G_Y_LTST-C155KGJSKT

PWRLED#-R

SUSLED#-R

LED2
LED_G_Y_LTST-C155KGJSKT

BATLED0# <22>

BATLED1# <22>

Q20
2N7002E

PWRLED#-R

R224

+3VO

10K_4

<22> PWRLED#

Q19
2N7002E

Q21
2N7002E

SUSLED#-R

R225

+3VSUS

10K_4

Q22
2N7002E

SUSLED#

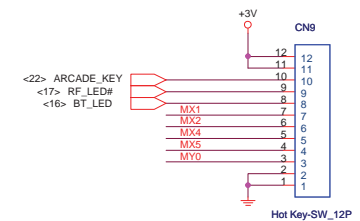
[illegible]

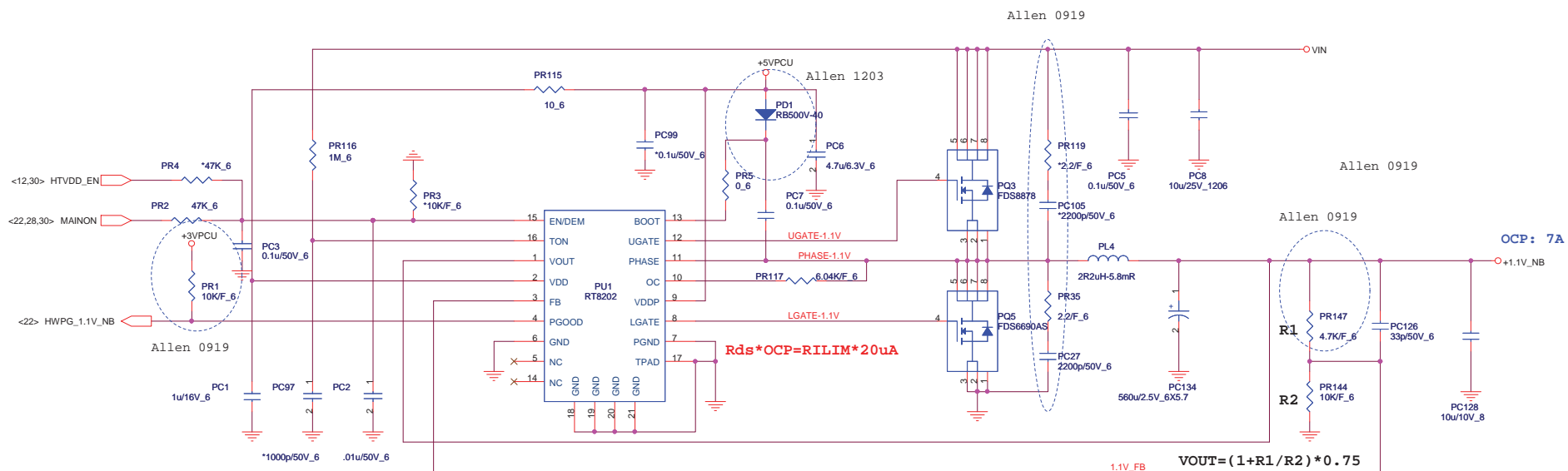
Pin 12 connection diagram for LED_CONN_12P. The diagram shows a 12-pin connector (CN3) with pins 1 through 12. Pin 12 is connected to +3VPCU. Pin 11 is connected to +3V. Pin 10 is connected to NBSWON#. Pin 9 is connected to CAPSLED#. Pin 8 is connected to NUMLED#. Pin 7 is connected to SATA_LED#. Pin 6 is connected to SUSLED#-R. Pin 5 is connected to PWRLED#-R. Pin 4 is connected to ground. Pin 3 is connected to ground. Pin 2 is connected to ground. Pin 1 is connected to ground. The label LED_CONN_12P is at the bottom.

Delete Debug Port(PCI & IDE)

BUTTON MATRIX

	MY0
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH





$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

$$FDS6690AS \text{ } R_{ds} = 12-15m\Omega$$


$$OCP = 7-0.8A$$

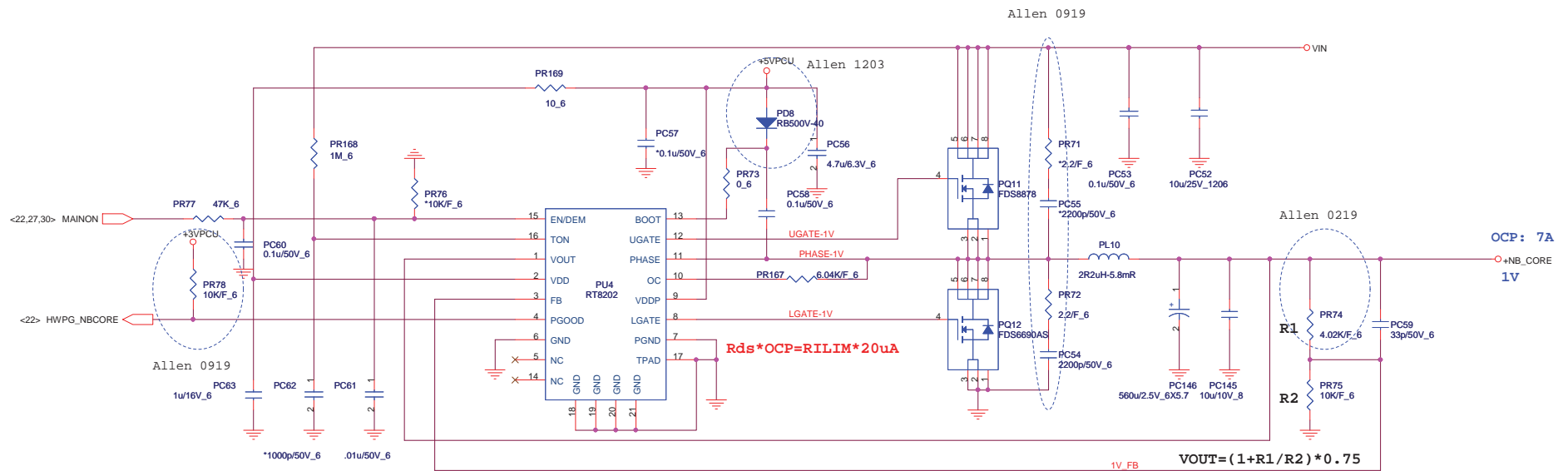
$$L(\text{ripple current}) = (19-1) * 1 / (2.2u * 272k * 19) \sim 1.58A$$

$$12m * 6 = RILIM * 20uA$$

$$RILIM = 3.6K (2.5-8K)$$

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		Quanta Computer Inc.	
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$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

FDS6690AS $R_{ds} = 12 \sim 15m\Omega$

OCP = 7 ~ 0.8A

$L(\text{ripple current})$

$$= (19 - 1) * 1 / (2.2u * 272k * 19)$$

$$\sim 1.58A$$

$$12m * 6 = RILIM * 20uA$$

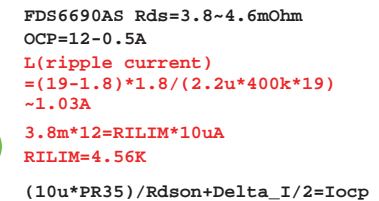
$$RILIM = 3.6K (2.5 \sim 8K)$$


<http://hobi-elektronika.net>

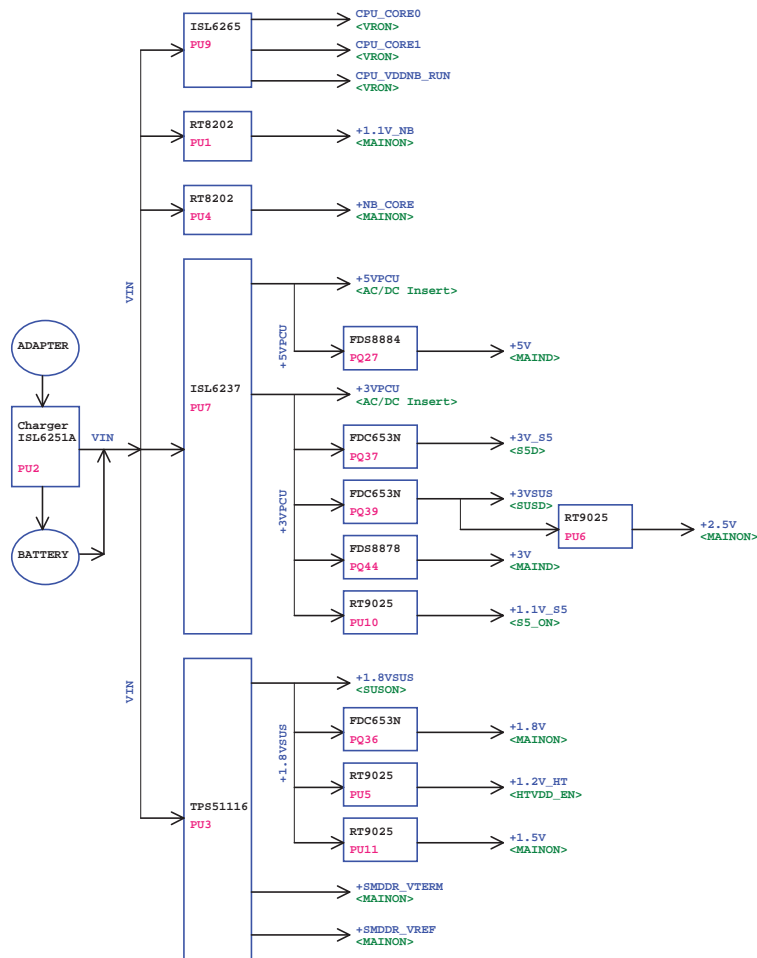


PROJECT : Z05
Quanta Computer Inc.

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	<p>PROJECT : Z05</p> <p>Quanta Computer Inc.</p>	
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1. +1.1V_S5MCP77M Power(+1.1V_DUAL)
2. +5VPCUPower IC VCC, USB PORT POWER(S3 control)
3. +5VAudio, FAN, Touch pad, SATA HDD, ODD, CRT
4. +3V_S5MCP77M, New Card, LAN Power
5. +3VPCUKBC WPCE755C,SPI ROM, LED, LID Switch, Fingerprint Module
6. +3VSUSBluetooth, Mini Card, MDC
7. +3VCPU Thermal Sense, MCP77M, System Memory, LCD Panel, PC Camera, Mini card, New Card, Audio, Codec, Card Reader, KBC WPCE775C, LED
8. +2.5VCPU VDDA
9. +3V_LANLAN Power(BCM5764M)
10. +1.2V_LANLAN Power(BCM5764M)
11. +2.5V_LANLAN Power(BCM5787M)
12. +1.5VMini Card, New Card
13. +1.8VSUSCPU VDD I/O, System Memory
14. SMDR_VTEMCPU Memory Interface , SYSTEM DDR DIMM Memory Termination
15. +1.8VMCP77M LCD Interface
16. +1.1V_NBMCP77M (HT Interface, PCI-E Interface, I/O Power, SATA Interface)
17. +NB_COREMCP77M Core Power
18. +1.2V_HTCPU HT Power
19. CPU_CORE0 CPU Power
20. CPU_CORE1 CPU Power
21. CPU_VDDNB_RUNCPU NB Power
- 22.